REMARKS

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 10-12, 14, 15, 18-20, 24, 25 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi, and further in view of Ommen.

Claims 10 and 24 include a package substrate having a thermally conductive substrate core and a buildup layer, having conductive traces and vias interconnecting top and bottom surface of the buildup layer, disposed only on a first portion of the substrate core and a heat spreader mounted to a second portion of a substrate core. Specifically, claims 10 and 24 include the limitations "a package substrate including a thermally conductive (or metal) substrate core, having first and second portions, and a buildup layer, including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the buildup layer, being disposed on only the first portion of the substrate core" and "a heat spreader mounted to the second portion of the substrate core."

Lischner does not teach or suggest a package substrate having a thermally conductive substrate core and a buildup layer being, having conductive traces and vias interconnecting top and bottom surface of the buildup layer, disposed only on a first portion of the substrate core and a heat spreader mounted to a second portion of a substrate core. Lischner teaches a circuit board assembly 100 with a flip chip package 110, having a heat spreader 140, connected to a printed circuit board 150 (Col. 2, lines 14-17). The first substrate 120 has a first surface 125 and a second

surface 126 (Col. 2, lines 19-20). The substrate may have a plurality of levels, which could be called buildup layers, with electrical paths between layers provided by interconnect vias 122 (Col. 2, lines 23-25). As clearly shown in Figures 1 and 3, these layers completely cover the substrate 120. There is no portion of a substrate 120 that is left uncovered by the buildup layers. Furthermore, the heat spreader as clearly shown in Figures 1 and 3 is attached to the buildup layers, not the substrate 120. Thus, Lischner teaches buildup layers completely covering a substrate core and a heat spreader attached to the buildup layers. Specifically, Lischner does not teach or suggest a package substrate having a thermally conductive substrate core and a buildup layer being, having conductive traces and vias interconnecting top and bottom surface of the buildup layer, disposed only on a first portion of the substrate core and a heat spreader mounted to a second portion of a substrate core.

Hiyoshi does not teach or suggest a package substrate having top and bottom buildup layers, with conductive traces and vias connecting a top surface to a bottom surface of the package substrate, disposed on a thermally conductive substrate core which has an exposed portion at a top surface thereof for attachment of a heat spreader. Hiyoshi discloses a semiconductor device having semiconductor chips 351-354 mounted on a ceramic substrate 31 with a circular flange 32 around a periphery of the substrate 31 (Col. 6, lines 48-55). Copper plates 331 and 332 are bonded to the top and bottom surfaces of the ceramic substrate 31 (Col. 6, lines 61-63). The copper plates 331 and 332 are made of a homogenous material and do not include conductive traces or vias. Hiyoshi thus does not disclose buildup layers.

Furthermore, as shown in Figure 2D, gate probe pins 471 and 472, along with conductive pillars 40, 41, and 45, extend away from the semiconductor chips 351-354 in a direction opposite the position of the copper plate 351 and do not interconnect top and bottom surfaces of the substrate on which the semiconductor chips 351-354 rest. Also, as shown in Figure 2B, the semiconductor chips 351 and 352 are connected to the emitter pedals 361 and 362 through metallic hemispheres 366. As is commonly understood in the art, metallic hemispheres, such as solder balls, are often used to electrically connect integrated circuits to other circuitry and devices, such as package substrates. However, as illustrated in Figure 2A, the metallic hemispheres 366 are on the sides of the integrated circuits 351 and 352 opposite the substrate 31. Thus, the substrate 31 is not being used as what is commonly understood to be a "package substrate" that interconnects integrated circuits with other devices such as circuits boards and sockets.

Therefore, Hiyoshi not only fails to disclose buildup layers, but actually teaches away from having buildup layers on the package substrate that include vias that extend therethrough. Specifically, Hiyoshi does not teach or suggest a package substrate having top and bottom buildup layers, with conductive traces and vias connecting a top surface to a bottom surface of the package substrate, disposed on a thermally conductive substrate core which has an exposed portion at a top surface thereof for attachment of a heat spreader.

Ommen does not teach or suggest a package substrate having top and bottom buildup layers, with conductive traces and vias connecting a top surface to a bottom

surface of the package substrate, disposed on a thermally conductive substrate core which has an exposed portion at a top surface thereof for attachment of a heat spreader. Ommen teaches a package capable of spreading heat from a semiconductor die (Abstract). As illustrated in Figure 1, pad array carrier package 10 is a semiconductor package, which comprises a heat spreader 11 having a first major surface 12 and a second major surface 13 (Col. 2, lines 33-37). Heat spreader 11 has a plurality of apertures or holes 16 extending therethrough and is coated with an electrically non-conductive adhesive material 17 which fills holes 16 (Col. 2, line 59 through Col. 3 line 7). The adhesive material 17 coats the first and second major surfaces 12 and 13 (Col. 3, lines 12-13).

An insulator layer 18 is formed on the adhesive material 17 and may cover the adhesive material 17 on both sides of the heat spreader 11 (Col. 3, lines 20-24). Top side conductive traces 20, bottom side conductive traces 24, and conductive pads 21 are formed on the insulator layer 18 (Col. 3, lines 51-55). A solder mask 26 is patterned over conductive traces 20 and 24 and over conductive pads 21 (Col. 4, lines 63-64). A protective metal cap 30 is bonded to the solder mask 26 using an adhesive material 27 (Col. 5, lines 7-8). The metal cap 30 serves as a heat spreader by promoting thermal conduction away from the semiconductor die 25 (Col. 5, lines 30-32). As clearly shown in Figure 1 the metal cap 30 is attached to the conductive traces 20 and 24 and conductive pads 21.

Ommen thus teaches conductive traces in pads disposed on a substrate core with a heat spreader attached to the conductive traces and pads. Specifically,

Ommen does not teach or suggest a package substrate having top and bottom buildup layers, with conductive traces and vias connecting a top surface to a bottom surface of the package substrate, disposed on a thermally conductive substrate core which has an exposed portion at a top surface thereof for attachment of a heat spreader.

Applicant respectfully submits that none of Lischner, Hiyoshi, and Ommen teaches or suggests a combination with either of the other two references. It would be impermissible hindsight based on applicant's own disclosure to combine Lischner, Hiyoshi, and Ommen. Additionally, as previously discussed, even if combined, Lischner, Hiyoshi, and Ommen fail to teach or suggest all of the limitations of claim 10.

Therefore, claims 10 and 24 are patentable over Lischner, Hiyoshi, and Ommen because claims 10 and 24 include a limitation that is not taught or suggested by Lischner, Hiyoshi, and Ommen.

Claims 11, 12, 14, 15, 18-20, 25, and 27 are dependent on either claim 10 or claim 24 and should be allowable for the same reasons as claims 10 and 24 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 10-12, 14, 15, 18-20, 24, 25 and 27 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi, and further in view of Ommen.

The Examiner has rejected claims 13 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi in view of Ommen, and further in view of Mertol.

Claims 13 and 28 are dependent on either claim 10 or claim 24 and should be allowable for the same reasons as claims 10 and 24 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 13 and 28 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi in view of Ommen, and further in view of Mertol.

The Examiner has rejected claims 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi in view of Ommen, and further in view of Hembree.

Claims 16 and 17 are dependent on claim 10 and should be allowable fore the same reasons as claim 10 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 16 and 17 under 35 U.S.C. § 103(a) as being unpatentable over Lischner in view of Hiyoshi in view of Ommen, and further in view of Hembree.

The Examiner has rejected claim 21 under 35 U.S.C. § 103(a) as being unpatentable over Kohara in view of Hiyoshi, and further in view of Ommen.

Claim 21 includes a package substrate having a thermally conductive substrate core, a buildup layer, having a plurality of conductive traces and vias interconnecting top and bottom surfaces of the buildup layer, being disposed on only a first portion of the substrate core, and a heat spreader mounted to a second portion of the substrate core. Specifically, claim 21 includes the limitations "a package substrate including a thermally conductive substrate core, having first and second portions, and a buildup layer, including a plurality of conductive traces and vias formed therein interconnecting top and bottom surfaces of the buildup layer, being disposed on only the first portion of the substrate core" and "a heat spreader mounted to the second portion of the substrate core."

Kohara does not teach or suggest a package substrate having a thermally conductive substrate core, a buildup layer, having a plurality of conductive traces and vias interconnecting top and bottom surfaces of the buildup layer, being disposed on only a first portion of the substrate core, and a heat spreader mounted to a second portion of the substrate core. Kohara teaches a semiconductor device including a flange 2 and flip-chips 6 mounted to a module base board 7. The flange 2 is also mounted to a heat sink 1 (Col. 5, lines 7-11). Kohara makes no mention of a package substrate with layers formed thereon. Specifically, Kohara does not teach or suggest a package substrate having a thermally conductive substrate core, a buildup layer, having a plurality of conductive traces and vias interconnecting top and bottom surfaces of the buildup layer, being disposed on only a first portion of

the substrate core, and a heat spreader mounted to a second portion of the substrate core.

As previously discussed, Hiyoshi and Ommen do not teach or suggest a package substrate having a thermally conductive substrate core, a buildup layer, having a plurality of conductive traces and vias interconnecting top and bottom surfaces of the buildup layer.

Applicant respectfully submits that none of Kohara, Hiyoshi, and Ommen teaches or suggests a combination with either of the other two references. It would be impermissible hindsight based on applicant's own disclosure to combine Kohara, Hiyoshi, and Ommen. Additionally, as previously discussed, even if combined, Kohara, Hiyoshi, and Ommen fail to teach or suggest all of the limitations of claim 21.

Therefore, claim 21 is patentable over Kohara, Hiyoshi, and Ommen because claim 21 includes limitations that are not taught or suggested by Kohara, Hiyoshi, and Ommen.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 21 under 35 U.S.C. § 103(a) as being unpatentable over Kohara in view of Hiyoshi, and further in view of Ommen.

The Examiner has rejected claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Kohara and Hiyoshi in view of Ommen, and further in view of Khandros.

Claim 22 is dependent on claim 21 and should be allowable for the same reasons as claim 21.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Kohara and Hiyoshi in view of Ommen, and further in view of Khandros.

The Examiner has rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Kohara in view of Hiyoshi in view of Ommen, and further in view of Mertol.

Claim 23 is dependent on claim 21 and should be allowable for the same reasons as claim 21 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Kohara in view of Hiyoshi in view of Ommen, and further in view of Mertol.

The Examiner has rejected claim 26 under 35 U.S.C. § 103(a) as being unpatentable over Lischner and Hiyoshi in view of Ommen, and further in view of Hembree.

Claim 26 is dependent on claim 24 and should be allowable for the same reasons as claim 24.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 26 under 35 U.S.C. § 103(a) as being unpatentable over Lischner and Hiyoshi in view of Ommen, and further in view of Hembree.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call **Mark A. Kupanoff** at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
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